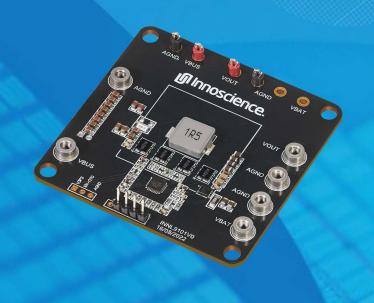


INNDDD150A1

Demo Manual 150W BUCK-BOOST

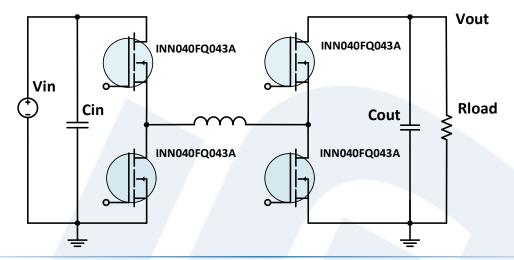




150W BUCK-BOOST

Four Switches Synchronous BUCK-BOOST

Input voltage 12Vdc-24Vdc, output 3.3V~19.2V/12A, maximum output power 150W, switching frequency up to 1200kHz, peak efficiency up to 98.1%.



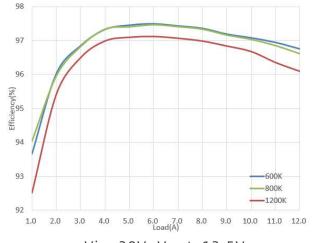
Highlighted Products

• INN040FQ043A

Target Applications

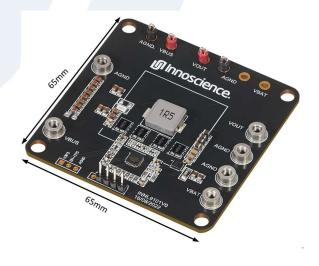
- Ultra-Books, Notebooks,
 Tablet PCs
- Car Charger

Test Results



Vin=20V, Vout=13.5V

Photo





List of Content

1. Overview	1
1.1.Description	1
1.2.Features	1
1.3.Applications	1
2. Parameters	2
3. Demo Solutions	3
3.1.System Solutions	3
3.2.Value of GaN	3
3.3.Highlighted Products	4
3.3.1. InnoGaN Device INN040FQ043A	4
4. Hardware Implementation	5
4.1.Photos	5
4.2.Design Considerations	5
4.2.1. Control IC	5
4.2.2. PCB Layout For Minimizing Parasitic Inductance	6
5. Testing & Results	8
5.1.Test Setup	8
5.2.Test Results	8
5.2.1. Efficiency curve	8
5.2.2. Switching Waveforms	10
5.2.3. Thermal Test	11
Appendix	12
Appendix A. Schematics	12
Appendix B. BOM	13
Appendix C. PCB Layouts	14
Revision History	16



1. Overview

1.1. Description

The INNDDD150A1 is a four switches synchronous BUCK-BOOST DC/DC module, which supports 150W output. The evaluation board features InnoGaN INN040FQ043A. The INNDDD150A1 operates from 12V to 24V input voltage range and generates adjustable 3.3V to 19.2V, 12Amax output. The switching frequency and dead time is adjustable for different evaluation scenario.

1.2. Features

■ Main features and Advantages

> High efficiency: 98.10% @ 24Vin, 19.2Vout/6A, 600KHz

> Adjustable switching frequency: 400KHz~1200KHz

> Adjustable output voltage: 3.3V~19.2V

■ Protection Function

- > Input over voltage protection
- > Input over current protection
- > Input over current protection

1.3. Applications

- Ultra-Books, Notebooks, Tablet PCs
- Car Charger



2. Parameters

Table 1 Electrical characteristics (Ta=25℃)

Symbol	Parameter	Conditions	Min	Nom	Max	Units			
System Specifications									
VIN	Input voltage		12	-	24	Vdc			
Fs	Switching frequency		400	-	1200	KHz			
VOUT	Output voltage		3.3	-	19.2	V			
POUT	Output power			150		W			
Demo Performance									
Eff,pk	Peak efficiency	Measured @Vin=24V, Output=19.2V/6A,600KHz		98.1		%			
Eff	Full load efficiency	Measured @Vin=20V, Output=13.5V/12A,600KHz		96.75		%			



3. Demo Solutions

3.1. System Solutions

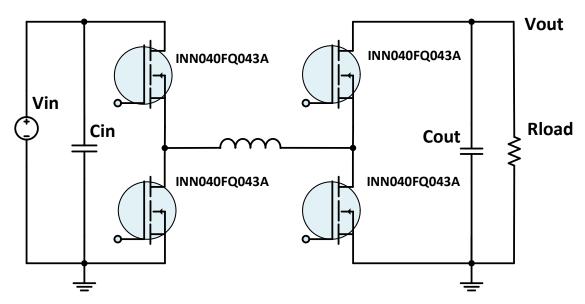


Figure 1 150W Demo board topology

The 150W BUCK-BOOST demo board adopts the solution of synchronous 4-switch BUCK-BOOST topology.

3.2. Value of GaN

Four GaN field effect transistors INN040FQ043A with FCQFN package, drain-source voltage 40V, and the maximum conduction resistance of $4.3m\Omega$ are adopted in the schematic.

■ Lower Driver Losses

The gate charge (Qg) of GaN is smaller, when the driver voltage is same, the driver loss for our GaN will be lower. Also, with same driver loss, GaN will allow higher frequency, which will reduce the size of another device.

■ Lower Switching Losses

The capacitance (C) determines the amount of charge (Q) that needs to be supplied to various terminals of the device to change the voltage across those terminals (Q = C*V). The parasitic capacitance of GaN is smaller, where Ciss and Crss are much smaller than Si MOSFET. The faster this charge is supplied, the faster the device will change voltage, and the less the switching time will be. So GaN has lower switching loss.



■ Zero Reverse Recovery

The reverse recovery charge QRR is a charge related to this reverse conduction mechanism, representing the amount of charge dissipated when a body diode is turned off. Reverse recovery charge does not directly relate to the device capacitances for an enhancement-mode GaN transistor. This charge comes from the minority carriers left over during diode conduction in a p-n junction of a MOSFET. Because there are no minority carriers involved in conduction in an enhancement-mode GaN transistor, there is no reverse recovery charge. Therefore, QRR is zero, which is a significant advantage compared with power MOSFET.

3.3. Highlighted Products

3.3.1. InnoGaN Device INN040FQ043A.

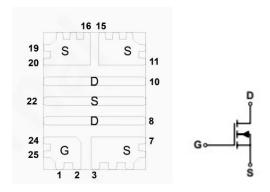


Figure 2 InnoGaN device INN040FQ043A

InnoGaN Device INN040FQ043A has FCQFN 3mm x 4mm package size, drain-source voltage 40V, and the maximum conduction resistance of $4.3 m\Omega$, compared with Si MOSFET 5mm x 6mm DFN package, INN040FQ043A has about 1/3 Ciss, 1/4 package size.



4. Hardware Implementation

4.1. Photos



Figure 3 Top view of INNDDD150A1

4.2. Design Considerations

4.2.1. Control IC

The control IC for the demo board is SC8886S from Southchip.SC8886S is a synchronous buck-boost charger controller, which supports buck mode, boost mode and buck-boost mode. SC8886S adopts Narrow-VDC power path management, which automatically regulates the current and voltage and controls the flow of power. SC8886S has 5.3V driver voltage which is suitable for GaN driving. Also, it supports different switching frequency from 400 KHz to 1200 KHz. Besides, it supports adjustable dead time from 10ns to 80ns.

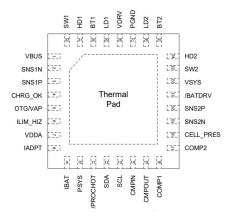


Figure 4 SC8886S top view



4.2.2. PCB Layout for Minimizing Parasitic Inductance

During PCB layout, great attention should be paid to the parasitic inductance, which includes CSI, power loop inductance and driver loop inductance as shown in Figure 5. The longer the trace, the greater the parasitic inductance will be. When a rapidly changing current flows through the device, an induced voltage will be generated across the common source inductor due to the blocking effect of the inductance. The induced voltage will cause the source and gate to ring, causing unexpected losses. As a result, we must minimize the parasitic inductance by optimized PCB layout.

For the power loop, place the high frequency bus capacitor as close to the two power switching devices as possible; for the driver loop, place the driver or controller close to the switching device so that the driver loop will be smaller. Besides, we can allocate the source pads closest to the gate to act as the "star" connection point for both the gate loop and power loop. The layout of the gate and power loops are then separated by having the currents flow in opposite or orthogonal directions, as shown in Figure 6.

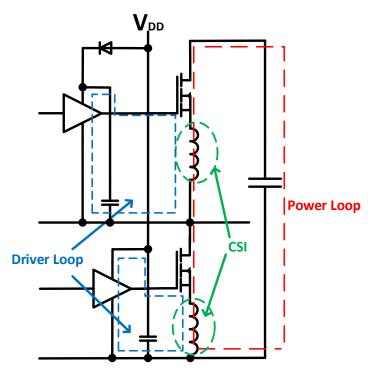


Figure 3 Schematic of half bridge power stage



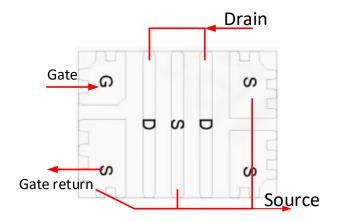


Figure 6 Minimize the common source inductance



5. Testing & Results

5.1. Test Setup

The 150W Buck-Boost demonstration board is easy to set up to evaluate the performance of INN40FQ043A.Before the test, we need to get all the equipment prepared, which includes DC source, electronic load, digital multimeter, and digital oscilloscope with 1 GHz bandwidth. Refer to Figures 4 and follow the procedure below for proper connection and measurement setup:

- a) With power off, connect the input power supply, load, digital multimeter and I2C interface according to figure 7 correctly;
- b) Turn on the input power supply to required value, make sure that input voltage does not exceed 26V.
- c) The default output voltage is 12.5V, and it can be set by host through the I2C interface, for more detailed

operation instructions, see Simple operation instruction.

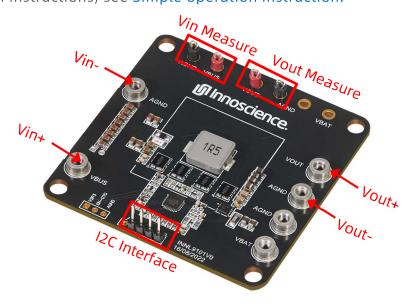


Figure 7 Example test connection

5.2. Test Results

5.2.1. Efficiency curve





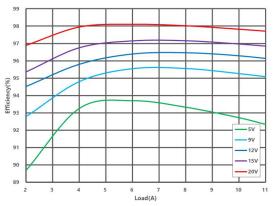
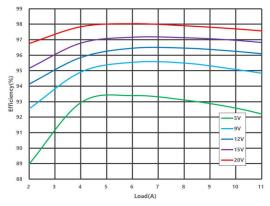


Figure 8 Efficiency Curve
Vin=20V, Vo=13.5V

Figure 9 Efficiency Curve Vin=24V, Fs=600KHz



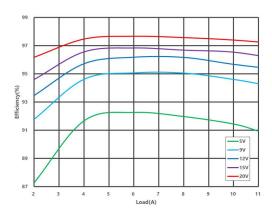
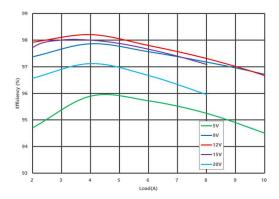


Figure 10 Efficiency curve Vin=24V, Fs=800KHz

Figure 11 Efficiency curve Vin=24V, Fs=1200KHz



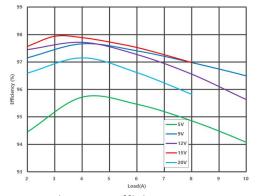


Figure 12 Efficiency Curve Vin=12V, Fs=600KHz

Figure 13 Efficiency Curve Vin=12V, Fs=800KHz



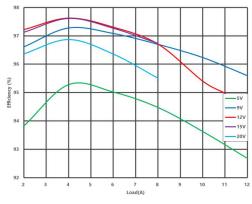
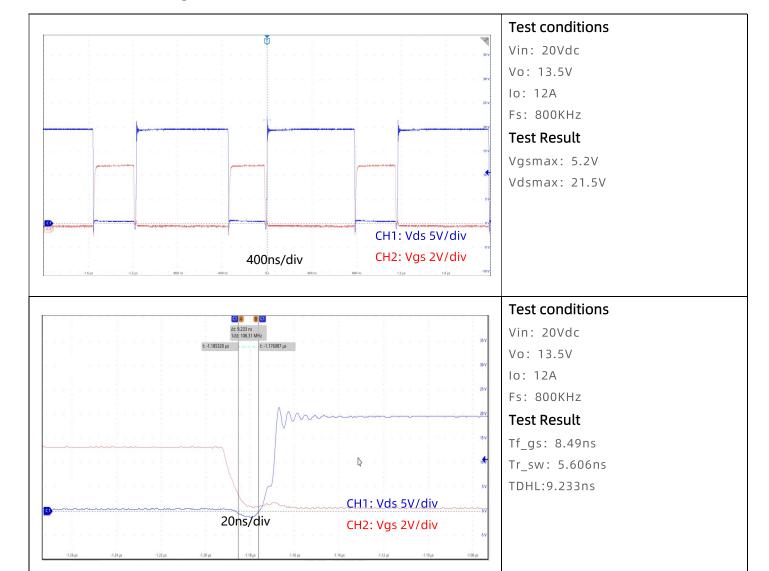
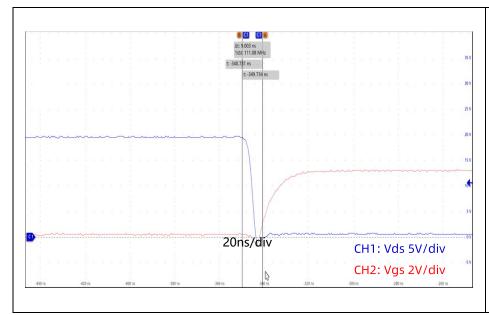


Figure 14 Efficiency Curve Vin=12V, Fs=1200KHz

5.2.2. Switching Waveforms







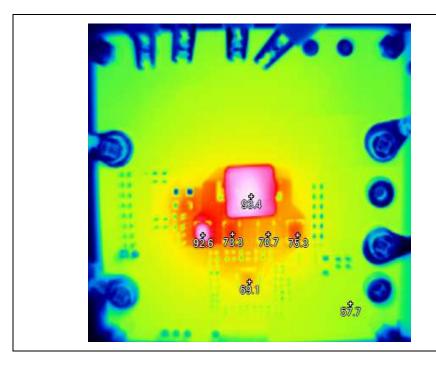
Test conditions

Vin: 20Vdc Vo: 13.5V Io: 12A Fs: 800KHz

Test Result

Tr_gs: 13.50ns Tf_sw: 3.115ns TDLH:9.003ns

5.2.3. Thermal Test



Test conditions

Vin=20Vdc

Vout=13.5V

lout=12A

Fs=800KHz

Ambient temp 25°C

Run for 1h

Result

Q2: 92.6°C Q3: 78.3°C Q4: 70.7°C Q1: 75.3°C

SC8886S: 69.1°C Inductance: 93.4°C



Appendix

Appendix A. Schematics

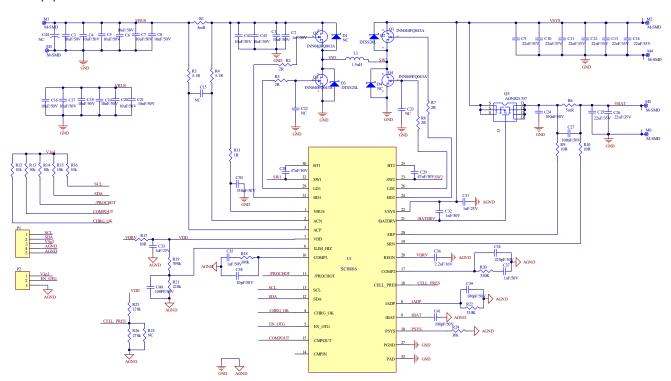


Figure 16 Schematic



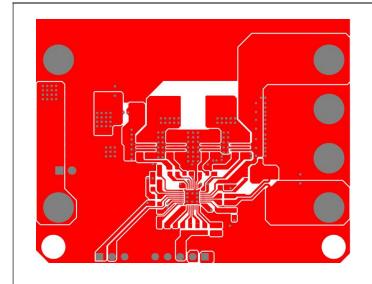
Appendix B. BOM

Table 2 BOM

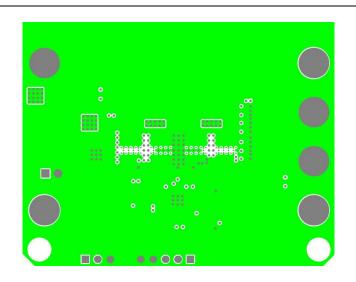
Comment	Description	Designator	Quantity
0603B103K500CT	10nF 0603 ±10% 50V X7R	C1	1
CL10B102KB8NNNC	1nF 0603 ±10% 50V X7R	C2, C32, C35, C37	4
GRM21BR61H106KE43L	10uF 0805 ±10% 50V X5R	C3, C4, C5, C6, C7, C8, C16,	14
C2012X5R1V226MT000E	22uF 0805 ±20% 35V X5R	C17, C18, C19, C20, C21, C42, C43	8
Capacitor	NC	C9, C10, C11, C12, C13,	3
CC0603KRX7R9BB104	100nF 0603 ±10% 50V X7R	C14, C25, C26	2
0603B473K500CT	47nF 0603 ±10% 50V X7R	C15, C22, C23	2
C1608X7R1H334KT000E	330nF 0603 ±10% 50V X7R	C24, C27	1
CL10B105KA8NNNC	1uF 0603 ±10% 25V X7R	C28, C29	2
GRM1885C1H221JA01D	220pF 0603 ±5% 50V NPO	C30	1
GRM188R61E225KA12D	2.2uF 0603 ±10% 25V X5R	C31, C33	1
GRM1885C1H100JA01D	10pF 0603 ±5% 50V COG	C34	1
CC0603JRNPO9BN101	100pF 0603 ±5% 50V NPO	C36	3
Capacitor	NC	C38	1
Schottky Diode	NC	C39, C40, C41	2
DTSS24L	40V 2A 420mV@2A	C44	2
MWSA1003S-1R5MT	1.5uH DCRmax=7.5mΩ	D1, D4	1
M3X5.56XL3+1.53	M3 chip nut	D2, D3	6
	Header, 5-Pin	L1	1
Header	NC	M1, M2, M3, M4, M5, M6	1
INN040FQ043A	40V 4.3mΩ@Vgs=5V	P1	4
AONR21357	30V PMOS	P2	1
STE1206M1W0R005FS	0.005R(5mR) 1206 ±1%	Q1, Q2, Q3, Q4	2
WR06W2R00FTL	2R 0603 ±1%	Q5	4
0603WAF510KT5E	5.1R 0603 ±1%	R1, R6	2
WR06X10R0FTL	10R 0603 ±1%	R2, R5, R7, R8	3
0603WAF100KT5E	1R 0603 ±1%	R3, R4	1
AF0603FR-0710KL	10K 0603 ±1%	R9, R10, R17	5
AC0603FR-07100KL	100K 0603 ±1%	R11	1
0603WAF3903T5E	390K 0603 ±1%	R12, R13, R14, R15, R16	1
0603WAF3303T5E	330K 0603 ±1%	R18	1
0603WAF2203T5E	220K 0603 ±1%	R19	1
0603WAF1303T5E	130K 0603 ±1%	R20	1
WR06X1203FTL	120K 0603 ±1%	R21	1
0603WAF3002T5E	30K 0603 ±1%	R22	1
	NC	R23	1
0603WAF2703T5E	270K 0603 ±1%	R24	1
SC8886S	IC Controller	R25	1
0603B103K500CT	10nF 0603 ±10% 50V X7R	R26	1
CL10B102KB8NNNC	1nF 0603 ±10% 50V X7R	U1	4



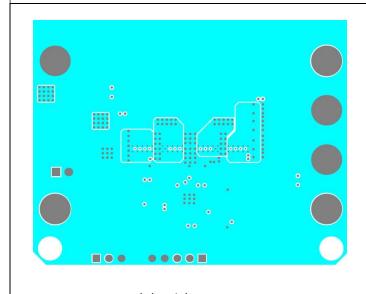
Appendix C. PCB Layouts



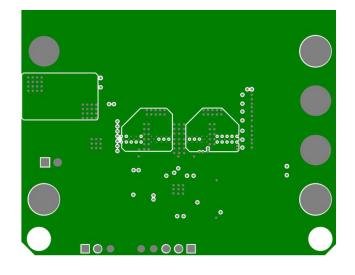
(a) Top Layer



(b) Mid Layer 1

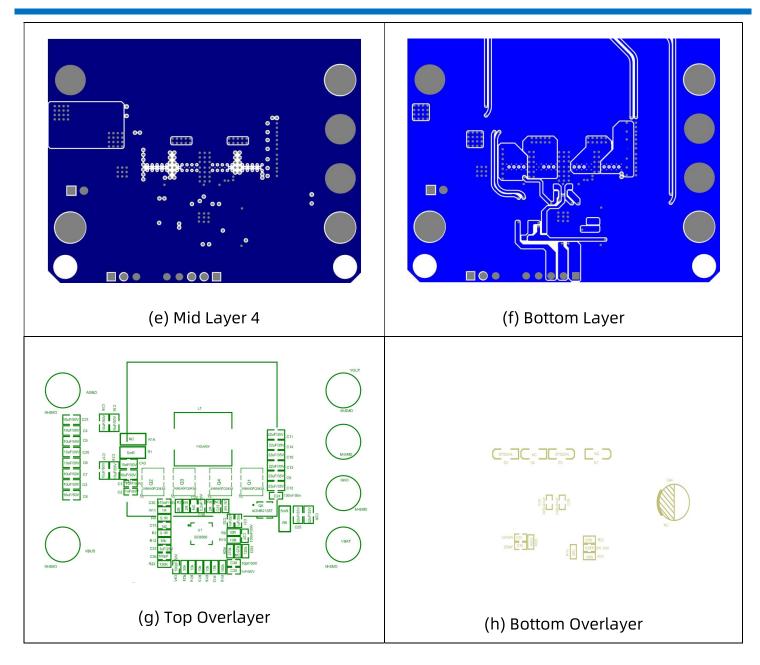


(c) Mid Layer 2



(d) Mid Layer 3







Revision History

Date	Author	Versions	Description	Check
12/9/2022	Zhanlai Yi	1.0	First edition	AE Team



Note:

There is a dangerous voltage on the demo board, and exposure to high voltage may lead to safety problems such as injury or death.

Proper operating and safety procedures must be adhered to and used only for laboratory evaluation demonstrations and not directly to end-user equipment.



Reminder:

This product contains parts that are susceptible to electrostatic discharge (ESD). When using this product, be sure to follow antistatic procedures.



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